# Experiment Name: Design and logic verification of combinational circuit of Y= C:\Users\Sarker\Desktop\bbveu.png using µ-wind

## Objectives:

* To implement AND,OR,INVERT gate
* Layout design simulation using Micro wind.
* To observe the deviation in results with default layout (automatic layout generation procedure) and our manual layout.

**Apparatus:**

**µ- wind software**

## Discription:

**The AND,OR,INVERT Gate:**

The truth-table and logic symbol with 4 inputs are shown below.

**The truth table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | Y=AB+CD |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

Schematic Diagram:

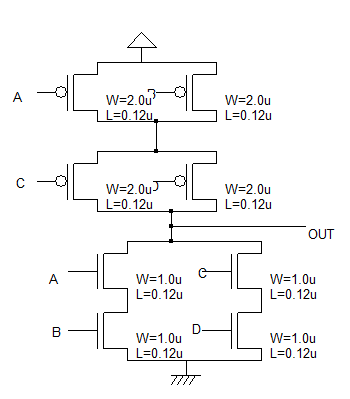
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Fig:Schematic Diagram

**Working Procedure:**

* The automatic layout generated is not optimal layout in terms of area. Nor does it fit in the library specifications that we want. So the next step is to design the layout manually.
* Use the layout editor to design a CMOS layout of our 4-input NAND gate. Attempt to minimize the width of the gate. Open microwind and click *File🡪Select Foundry* and select *cmos 025.rul*. this sets our layout editor designs 0.25u technology.

* Let us consider the problem specifications are 100 lamda height and 20 lamda for Vdd and GND rails. So we will place Vdd and GND rails 20 lamda height and spaced 60 lamda apart. Vdd and GND rails are in Metal. The top rail is used as Vdd. And the buttom one is as GND. To create a metal rectangle click on Metal 1 in the palette and then the required rectangle in the layout window.

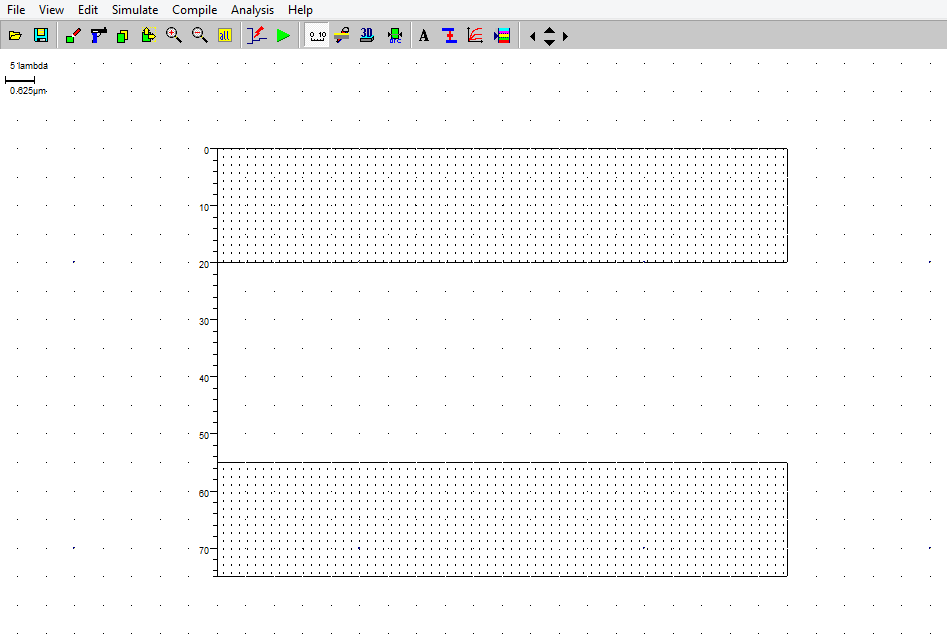
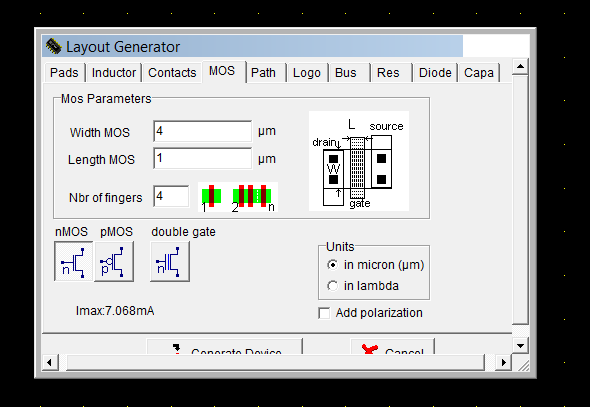


Fig1: Layout design

* The next step is to build nMOS transistors. These are in series for a NAND gate. Click on the transistor symbol in the palette. A layout generator window will appears. Click on MOS tab and set W, L of the transistor. Set the type (nMOS/pMOS). Check the units of the sizes (lamda/micron).



* Then click on generate device and place it in the layout. Now place the nMOS transistor on the layout close to to the GND rail on the top. To contract two nMOS in series, the diffusions are shifted to a side and another poly line is addred as second transistor. Once again, the diffusion is shared to save area to reduce capacitance. In the figure below the n-diffusion in the nMOS transistor is stretch to the left and a second copy line is added. To add a poly line click on the polysilicon in the pelette and create the required size rectangle in the layout window.

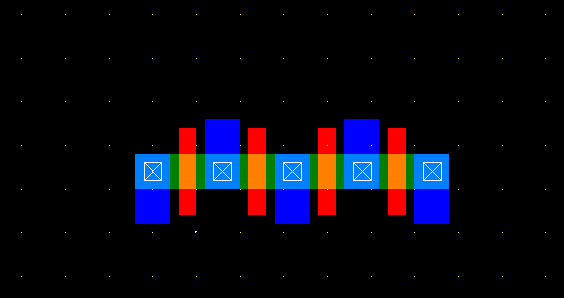
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Fig3: nMOS added.

* The next step is to place two pMOS transistor in parallel. The source of the transistor is connected to the Vdd to the top. Create another device in a similar manner to place it in parallel to the first pMOS device. We share the 4 devices drain diffusions. This saves on area as well as reduces capatences. At any stage of designing the layout, we can run DRC check to see if your design has any errors. A DRC check can be run by clicking an Analysis🡪 Design Rule Checker.

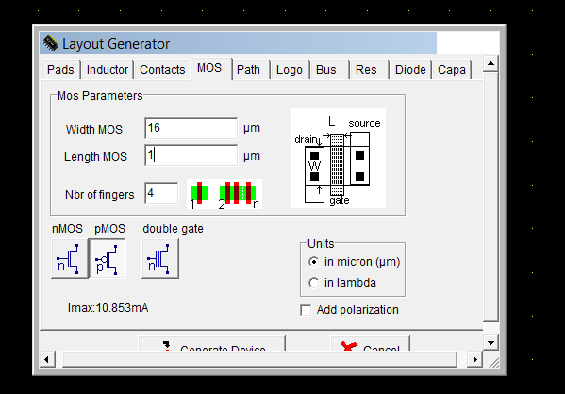


Fig 4:Adding pMOS

* Place the pMOS transistor in our design.

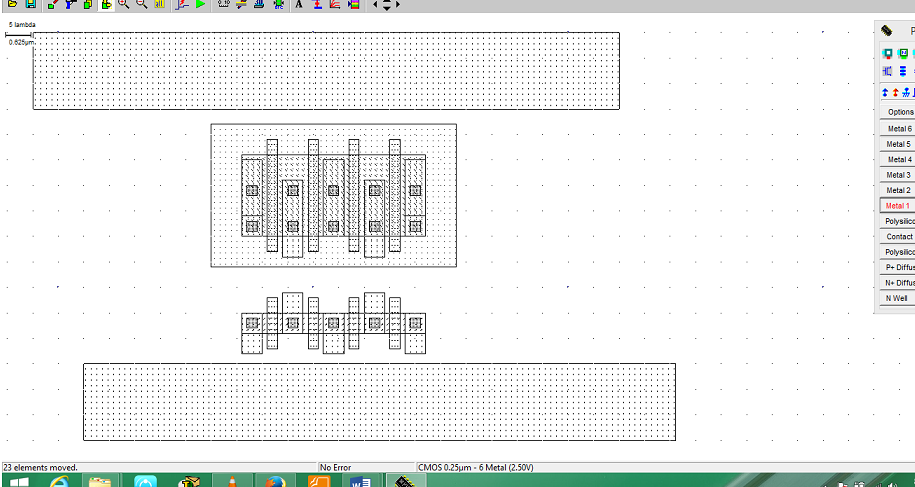


Fig 5: pMOS added

* Now metal and poly inputs are connected.

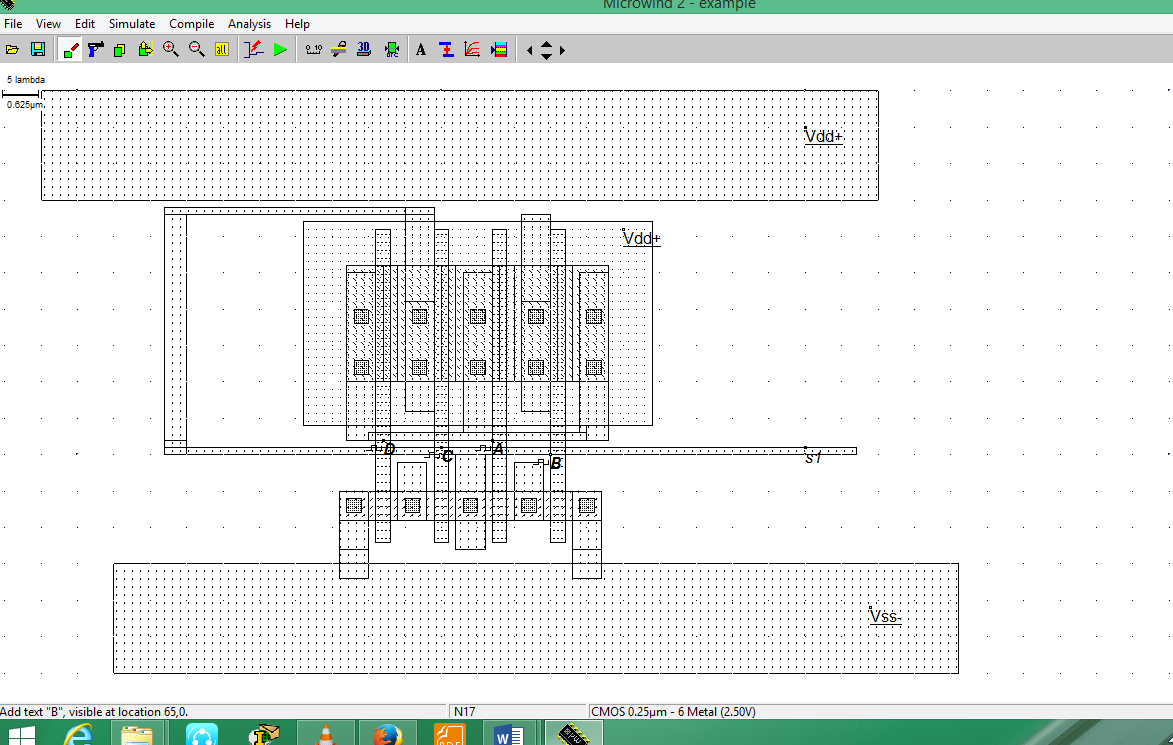


Fig 6: adding poly silicon connections

* Finally the input and output are connected and we are now ready to run the simulation.

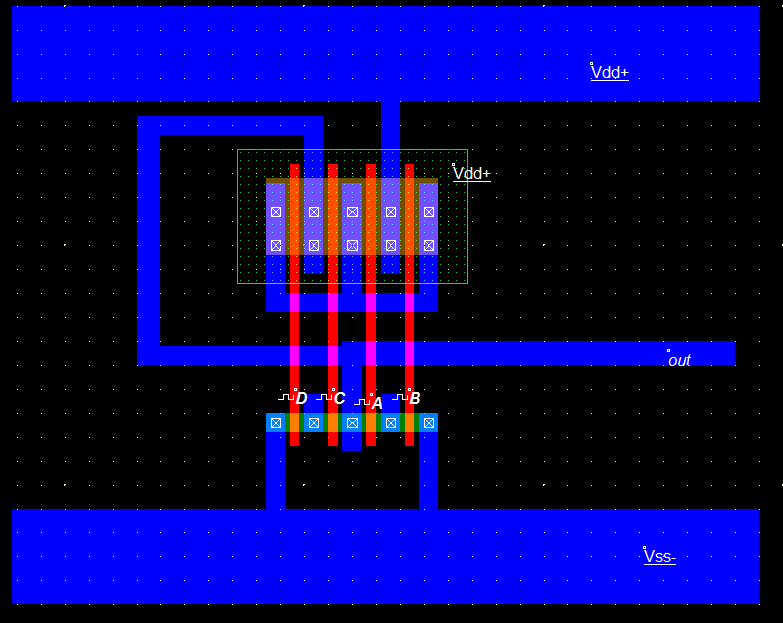


Fig 7: final diagram of compounf gate(AND,OR,INVERT)

* To run the simulation of our circuit, click on *Simulate🡪Start Simulation.* Depending on the input sequences assigned at the input the output is observed. The power value is also taken. Make tphl, tplh and tp measurements, by changing the input sequences and clicking and dragging the mouse on the waveform in the horizontal direction. Most of the times, microwind automatically provides with the rise and fall delays on the waveforms. The power consumption is also provided at the bottom right of the window.

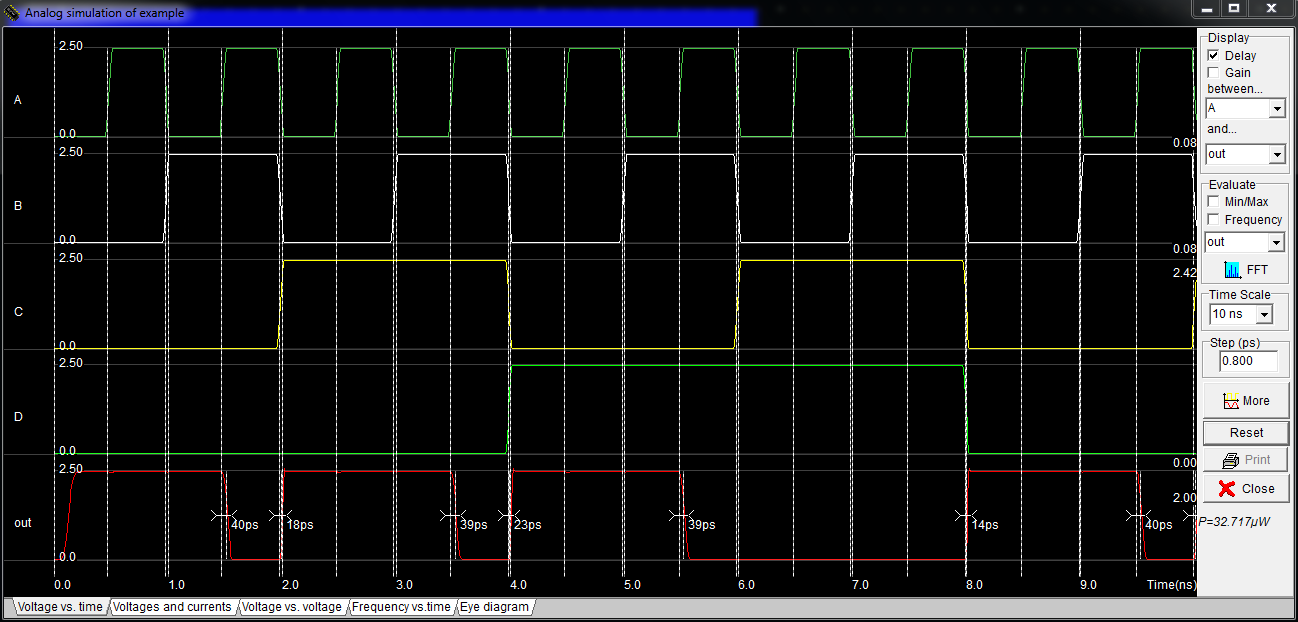


Fig 8: Timing diagram

### Conclusion:

The AND,OR,INVERT gate is implemented using two pMOS and two nMMOS and the truth table is successfully verified. The required waveforms were obtained, observed and noted down using microwind2.